



REV	DATE	DESCRIPTION
1,2001_04-2	Sept. 2004	1. Initial design files 2. J.2. Diagnostic Distribution Review (entry) 3. Package PCB mounting holes 4. Backplane PCB with AXE 5. Full PFD Postprint, 6. Dimension and Millen 6. Add SW menu for 10 and 20 7. Add SW menu with MCL, Interrupt based option 8. Relate J104, MDT output 9. 8001 Change with MCL, Interrupt based option 10. Add Top Panel - +12 V, Power Supply 11. Inverter added to Panel 12. Revised Panel to: Backlighting - 1, Analog - 2, Channel - Channel1 13. Add MDT Power Switch 14. Add Hardware for Power and USB Penetration 15. Label J107 as External Switch 16. CPU and CPU was updated after Memory address change. 17. U1 and U11 has been updated to 08FAU010D

REV	DATE	DESCRIPTION
1,2001_04	Jan. 2004	Release with USB and analog clock
1,2001_04	March 15, 2004	Postprint Rev
1,2001_04	March 17, 2004	SW Check (New-Release)

1. DURING DATA TRANSMISSION, DATA FLOW IS FROM UP THROUGH PFD, INTO DLP USB THROUGH READ SW SWITCH TO UP UP OUTPUT IS TRI-STATED.

2. DATA RECEPTION IS FROM DLP USB THROUGH READ SW SWITCH TO UP UP OUTPUT IS TRI-STATED.

NOTE: When USB cable is connected, always check connection. Always make connection from the USB cable correct when USB is open.

NOTE: Use the pin base from USB cable, no modification. Always make USB cable correct when USB is open.

**NOTES:**

- BOARD PIN IS 741621 REV.0
- UNLESS OTHERWISE NOTED:
  - RESISTORS ARE 1% TO 5% TOL.
  - CAPS W/O TOLERANCE ARE 5% TOL.
  - DATA IS UNLESS INDICATED OTHERWISE
- COMPONENT PART NUMBERS ARE SHOWN FOR INFORMATIONAL PURPOSES ONLY. CHECK PARTS LIST FOR ACTUAL VALUES
- PARTS LIST GENERATOR:
  - Item: Quantity (B) Reference (A) Value (P) Part (P) Package (P) Qty (P)